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6T SRAM cell design using CMOS transistor and CNTFET

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***Abstract*— Static random access memory (SRAM) is a crucial component of embedded systems. Due to the large storage density and less access time of the SRAM cell, it has become major data storage device in an embedded system. As the demand rises for low voltage, high speed and low power devices, 6T SRAM cell is proposed in 45 nm technology node. Therefore, SRAM cell is designed and implemented in both CMOS [1, 2] and CNTFET devices. In this paper, SRAM operation is evaluated in two metrics, first one is by design metrics which includes the calculation of power dissipation, delay and the calculation of power delay product. Power delay product is also called as switching energy because it provides the information of the energy consumption in a switching event. Second one is by stability metric in which the analysis is done in two ways, one is by measuring the static noise margin and another is by the N_curve metric.**

Keywords—SRAM, CMOS, CNTFET, Static Noise margin, write trip power, N_curve metrics, Stability Analysis, Write Critical current.

I. INTRODUCTION

Basic SRAM cell contains 6 transistors. SRAM cell circuit diagram is shown in Figure 1. An SRAM column usually contains more than one cell depending on the supplementary circuitry. Supplementary circuits are used for efficient operation of memory cell during read and write operation. The basic SRAM cell is constructed by two back to back connected inverters and two access transistors. Each SRAM cell column contains pre-charge and write circuitry where the sense and read circuitry is shared by several columns. During idle state, the pre-charge signal is high; thus bit-line voltages are pre-charged to V_{dd}. Pre-charge is turned low before read/write operations [3].

SRAM cell is designed using CNTFET. CNTFET is an alternative for silicon based technology that does not have MOSFET problems such as drain induced barrier lowering, threshold voltage roll off, punch through effect, thermal run away and many more when the MOSFET is subjected to ultra scaling. Hence to eliminate these problems from MOSFET many more technologies have been evolved such as CNTFET, SETs, QCA and Benzene ring technology etc. From these CNTFET stands first due to its robustness and electrical property [4, 5].

Circuit diagrams of SRAM cell using CMOS and CNTFET are shown in figure1 and 2.The 6T SRAM cell is consist of 6 Transistors where 4 transistors are coupled as inverter, here bit is stored as 1 or 0 and other two transistor is act as access transistor to control the SRAM cell by bits line. When WL (word line) is high then the SRAM cell can be accessed [3].

There are three basic operations in SRAM memory cell. They are read, Write and Hold operations.

(i) Read operation: In read mode, world line WL is activated to enables the two access transistors which are connected to the bit lines BL and BLB. The data stored at node Q and QB are passed to the bit lines in read operation. In read mode, BL and BLB acts as output lines and Q and QB acts as input lines. Let us assume that the stored data is "1" at the node, which has to be read at BL. If Q is high and QB is low, keep the WL to be high to perform the read operation, As Q=1, there is no discharge in the circuit because there is no voltage difference between Q and BL. As QB=0, there will be a voltage difference between the QB and the node voltage at BLB. Therefore, there will be discharge in the circuit and current flows. The BLB will discharge through N2, and BL is pulled up through P1 to V_{DD} (refer figure 1). In read operation P2 and N1 transistors are turned off but the transistors N2 and P1 are operate in linear mode. In this manner, the data is read at BL in SRAM cell.

Let us assume that, the stored data is "0" which has to be read at BL. If the stored data is "0", then the internal nodes Q=0 and QB=1, when the WL=1, as QB is high, there is no voltage variations between the nodes so there is no discharge in the circuit. As Q is low, there is voltage difference between the nodes Q and BL, so there is a discharge in the circuit at Q and BL. The transistor must have the ratio such that Q lies below the threshold region of P2/N2. This is the constraint in the read operation. As bit voltage decreases, the output is "0".

(ii) Write Operation: In write operation, bit lines BL and BLB are considered as input lines. The word line WL is at V_{DD} to perform the write operation. As we have control on the bit lines, initially connect BLB to ground to develop the voltage difference between QB and BLB. To write "1" onto the SRAM cell, N2 must be stronger than P2 to provide the discharge path. This can be achieved by changing the aspect ratio of the transistors.

(iii) Hold Operation: In hold mode, word line WL is connected to ground potential to turn OFF the access transistor

N3 and N4. So, the SRAM cell cannot be accessed and the stored data remain same as long as the access transistors turned ON or the supply voltage exists.

SRAM operation is evaluated in two metrics

A. Design Metrics

1. Power Dissipation*:* For portable devices long battery life and the satisfactory performance are required. To achieve this, the power dissipation of the circuit should be minimized. There are two types of power dissipation; one is static power dissipation and dynamic power dissipation. The addition of these two power dissipation referred as total power dissipation [6]. If the system is in standby mode, Static power dissipation occurs. During read and write operation, the power consumed from the system is referred to as dynamic power dissipation. The product of current consumed from the source and the voltage consumed from the source is called as power consumption [7]. Now a day, an electronic device requires design with low power dissipation. The dynamic power dissipation limits the technology scale down.

2. Delay: Delay is the difference between time at which the input is applied and the time at which the output is obtained. To increase the system speed, the design is designed with less delay. The read access time and the write access time of the SRAM cell measures the speed of the cell.

3. Power Delay Product: Power delay product (PDP) is used to measure the switching energy of the system because it represents the energy consumed during switching event, i.e. from low to high and high to low transition. As the name suggests that, it is the product of average power consumption and the delay of the system. The circuit with low power delay product is considered as the energy efficient circuit [8].

B. Stability Metrics

Stability of the SRAM cell can be analysed using two metrics named as SNM metric and N-curve metric.

a) Static Noise Margin. Static Noise Margin helps to determine the stability of the SRAM [6, 7].The least noise voltage needed to change the cell state is SNM [9]. Butterfly curve is one of the method to calculate the Static Noise margin [6]. Butterfly curve is plotted by drawing and mirroring the inverter characteristics and then finding the maximum possible square between them [6, 7, 10]. SNM is the sides length of the square which is plotted on the butterfly curve. Greater the SNM better is stability.

1) Static Noise Margin in Hold Mode. In absence of word line voltage, the ability of SRAM to retain the stored data is defined as hold stability. SNM in HOLD mode is measured as shown in Figure 3 using butterfly curve [11]. The dashed line in Figure 3 denotes that there is no connection between the circuits.

2) Static Noise Margin in Write Mode. The minimum voltage required to feed new value into the SRAM cell is known as write margin [7].Write stability is the ability of the SRAM to allow the changes in the stored value. Figure 4 shows the schematic for the calculation of SNM using the butterfly curve method in the write mode of SRAM.

3) Static Noise Margin in Read Margin. The read margin is used to find out read stability of the SRAM. Read Stability is the ability to prevent the SRAM cell to flip the stored value while the stored value is being read [7]. Figure 5 shows the schematics for the SNM measurement using the butterfly curve method in the read mode of SRAM [11].The value of SNM is least during the read operation which means the SRAM is most vulnerable during read operation [12].

b) N-Curve Metric:

This method is used to check the stability of the SRAM Cell. This technique is the replacement of the SNM technique, because the SNM technique is error prone and time consuming methods and the proper adjustment of the square in VTC is difficult and not possible to fix the square accurately. Hence, to overcome the drawbacks of the SNM Technology, N_curve metric is used for the stability analysis of the SRAM cell. The N_curve metric will also provide the supplementary statistics about the SRAM Cell stability and write ability. In addition to that, it also gives the information about the voltage and current in a single plot which helps intern to measure the power of the SRAM Cell which will be helpful for the SRAM analysis for better circuit design.

The factors affect the stability of the SRAM cell are Pull-up Ratio (PR), Cell Ratio (CR), Supply Voltage, Temperature, Technology variation such as threshold voltage variations, diameter variations and many more.

• ***Pull-up Ratio*****:** Pull-up ratio determines the write margin [14]. As pull up ratio increases, WSNM of the SRAM cell reduces, therefore beyond certain limit pull up ratio should not be increased [15]. For better WSNM of SRAM cell the pass transistors N3 and N4 should be stronger than the PMOS device or PCNTFET which are called as pull up transistors.

• ***Cell Ratio*****:** Cell ratio determines the read margin. To get higher RSNM, the cell ratio should be larger. Therefore, for better SNM strong pull down transistors N1 and N2 and weak pass transistors are preferred.

• ***Supply Voltage*****:** When the supply voltage is scaled down close to the V_{th}, the speed of the read operation, read and write margin are reduces significantly. Mainly read operation become destructive. Hence proper maintenance of Supply voltage is very important which should not be close to the threshold voltage.

•***Temperature*****:** As the temperature increases, the speed of the SRAM cell increases due to the mobility of the charge carriers variation but the stability of the SRAM cell reduces thus reduces the SNM of the SRAM Cell [16].

• ***Technology Variation:*** Threshold voltage of the device varies when the device dimension reduces, thus leading to fluctuation of intrinsic process parameters such as random dopant density variation in channel, drain and source which affects SRAM cell stability and write time [15] which intern reduces technology scaling reduction to 45nm, 22nm and 16nm nodes.

Stability Analysis of SRAM using N_Curve Metrics:

Using N_curve metrics, the stability of the SRAM cell can be analyzed as follows:

1) Read Stability: The stability of read operation can be obtained by bringing out the read N- curve. To get N_curve metric during read operation the bit-lines are connected to V_{dd} and the word-line is activated. Then, a voltage sweep of Vin from 0V to V_{dd} was applied at the node QB assume it is storing a "0" to obtain the corresponding current I_{in}.

2) Write Ability: The ability of write operation can be obtained by using the N-curve during write operation. It is same as that of the read N-curve except that one of the bit lines, that is BLB or BL depending on where the dc supply is attached, is connected to ground instead of V_{dd} [17]. Subsequently, dc sweep is performed on the internal node QB; the write N- curve will provide the critical current (I_{CRIT_WR}) which is the required and minimum current for write operation to write data into the cell without absorption.

3) Static Voltage Noise Margin (SNVM): It is the highest bearable DC noise voltage at the input of the inverter of the SRAM cell before changing its content. The variance between A and B in figure 6 shows highest bearable DC noise voltage before swapping of cell content [17].

$$SVNM = V_B - V_A \ldots\ldots\ldots\ldots\ldots\ldots (1)$$

4) Static Current Noise Margin (SIVM): It is the highest bearable DC current that can be introduced into the cell before changing its content and it is measured as a highest current located between point A and B. The SINM is used to indicate the stability of the memory cell [17, 18].

5) Write Trip Voltage (WTV): The write ability of the memory cell can be analysed using write trip voltage. Write trip voltage is the lowest voltage drop required to change the internal node to "1" of the SRAM cell when both bit lines are connected to V_{dd}. Therefore, it can be measured as a variance between point C and B as shown in figure 6 of the simulation result[17, 18].

6) Write Trip Current (WTI): It is used to analyse the write ability of the memory cell. It is the lowest amount of current required to write the data into the cell and it can be measured as a negative peak current between the points C and B as shown in the N-curve of figure 6 during read and hold operation. If there is any crossing of points A and B or point B and C occurs, that shows that there is loss of stability of memory cell [17, 18].

7) Static Power Noise Margin (SPNM): It is the multiplication of the SVNM and SINM. If SPNM is large, better stability can be achieved [18]. It is extracted from the area below the curve between point A and B. And it can be expressed by the equation,

$$SPNM = \sum_A^B Iin * Vin \ldots\ldots\ldots\ldots (2)$$

8) Write Trip Power (WTP): To achieve better write ability WTP should be large [18]. It is extracted from the area below the curve between point C and B. Also, it can be expressed by the equation,

$$WTP = \sum_B^C Iin * Vin \ldots\ldots\ldots\ldots (3)$$

Where Vin is the sweep voltage source and I_{in} is the current supplied by the sweep voltage Vin. Therefore, for successful read and write operation static power noise margin must be positive while write trip current must be negative [18].

A. Simulation Results

SRAM Cell is designed and implemented using CMOS transistor and CNTFET. The Simulation result consists of the Power, delay and power delay product of the SRAM cell using both CMOS transistor and CNTFET has been evaluated and tabulated the result in table I. Power delay product is the important to compute the energy consumption of the SRAM Cell.

The stability analysis of the SRAM cell is obtained using butterfly curve and N_curve metrics under process variation such as CR, PR for the 6T SRAM cells constructed using both MOSFET and CNTFET. The cell ratio and pull up ratio can be calculated using the aspect ratios of the ON transistors of the SRAM cell during read and write operations respectively. The result of SNM in all three modes of operation is tabulated in the table II. To get the better SNM and to find the write trip current, voltage and power, N_curve metrics analysis have been done and the results are tabulated in the table III.

C. FIGURES AND TABLES

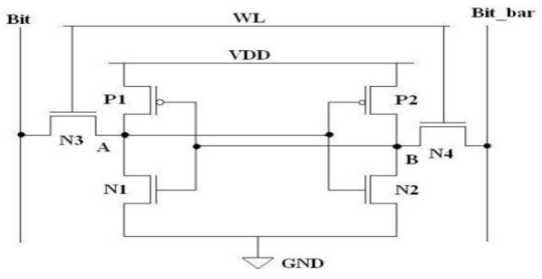

Figure 1: Circuit diagram of 6T SRAM Cell using CMOS transistors

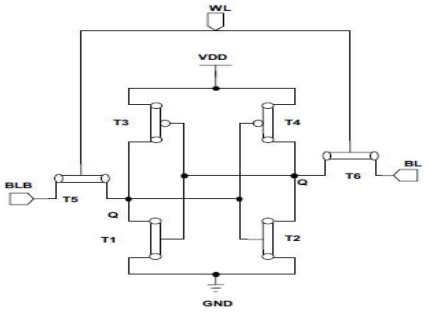

Figure 2: 6T SRAM Cell using CNTFET

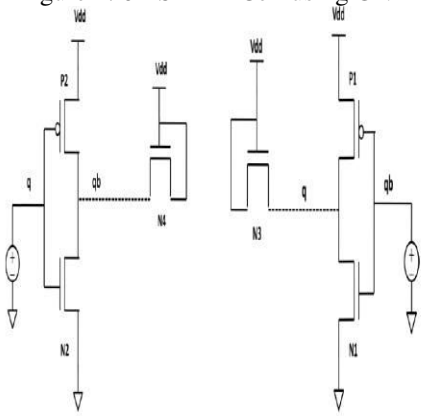

Figure 3: Schematics to find the static noise margin in HOLD Mode.

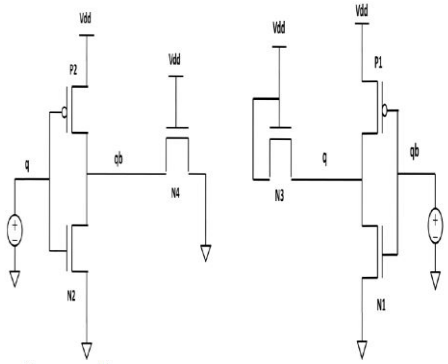

Figure 4: Schematics to find the static noise margin in WRITE Mode.

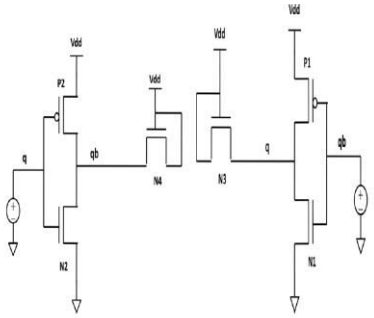

Figure 5: Working path of RSNM

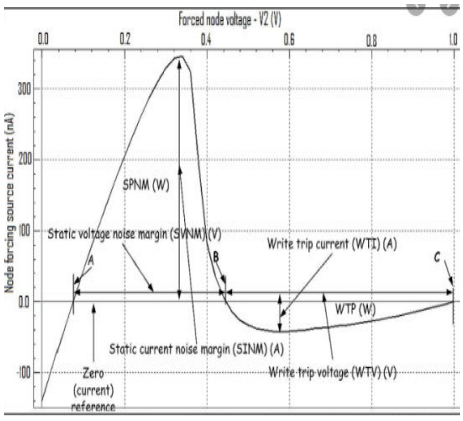

Figure 6: N_curve metrics

Table I: Power and delay calculation

Device	Static Power	Dynamic power	Total Power	Delay	PDP
MOSFET	2.028168nW	51.4939 µW	51.4959 µW	11.1671ns	575.06f
CNTFET	113.30676 µW	111.72053 µW	1.58623 µW	40.5635ps	0.06434f

Table II: Static Noise Margin Analysis

Device	HSNM	RSNM (CR=3.33)	WSNM (PR=1)
MOSFET	0.44	0.41	0.16
CNTFET	0.47	0.123	0.11

Table III: Analysis of SRAM Cell using N-Curve for HOLD, READ and WRITE operations.

Device	HOLD								
	V_A in V	V_B in V	V_C in V	SVNM in V	SINM in A	WTI in A	WTV in V	SPNM in W	WTP in W
MOSFET	126m	710m	--	584m	434.023µ	-96.3µ	--	253.47µ	--
CNTFET	0	901.137m	0	901.137m	60.09µ	-59.22µ	-901.137m	54.15µ	--
Device	READ								
	V_A	V_B	V_C	SVNM	SINM	WTI	WTV	SPNM	WTP
MOSFET	220.5m	762.42m	--	541.92m	354.93µ	-81.274µ	--	192.34µ	--
CNTFET	0	--	--	0	20.594µ	-20.876µ	-		
Device	WRITE								
	V_A	V_B	V_C	SVNM	SINM	WTI	WTV	SPNM	WTP
MOSFET	--	--	--	--	--	--	--	--	--
CNTFET	0	--	--	--	130.911µ	69.1µ	--	--	--

D. Conclusion

6T SRAM cell has been designed in 45 nm technology using MOSFET and CNTFET. Calculated the delay, static power, dynamic power, total power, PDP for each 6T SRAM in 45nm technology. Static noise margin and the N_curve metric were used for stability analysis of the SRAM cell. As per the simulation results shown in table I, CNTFET gives the less PDP than the CMOS transistor, which shows that the energy consumed by the CNTFET SRAM cell is less than the CMOS transistor SRAM cell. From table II, in hold mode stability of the CNTFET SRAM cell is more than the CMOS transistor SRAM Cell and also stability of the CNTFET SRAM is more than the stability of the CMOS transistor SRAM cell in read SNM. The write stability of the CNTFET SRAM cell is more than the CMOS SRAM cell, that can be observed in the table III. The I_{CRIT_WR} of the CNTFET SRAM cell is 69.1µA which is minimum and necessary current for the SRAM to write the data into cell. Further work to be carried out to get the more stability in write and read mode. There is a future scope to get the better response by consider some of the parameter variations of CNTFET.

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